REMARKS

Claims 1-53 are pending. Claims 1, 9, 16, 24, 31, 39, and 48 have been amended. No new matter has been introduced. Reexamination and reconsideration of the present application are respectfully requested.

As requested in the accompanying Change of Address Notice, please direct all future communications regarding this application to: Roger R. Wise, Esq., PILLSBURY WINTHROP LLP, 725 S. Figueroa Street, Suite 2800, Los Angeles, CA 90017-5406, telephone (213) 488-7100, facsimile (213) 629-1033.

In the February 13, 2003 Office Action, the Examiner rejected claims 1-53. The Examiner rejected claims 9, 10, 15, 24, 25, and 30 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,182,257 to Gillingham (the Gillingham reference). The Examiner rejected claims 1, 2, 7, 8, 16, 17, 22, and 23 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, in view of U.S. Patent No. 6,477,674 to Bates et al. (the Bates reference). The Examiner rejected claims 3 and 18 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference and the Bates reference, and further in view of U.S. Patent No. 5,638,382 to Krick et al. (the Krick reference). The Examiner rejected claims 4 and 19 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, the Bates reference, the Krick reference, and further in view of U.S. Patent No. 4,837,785 to McAlpine (the McAlpine). The Examiner rejected claims 5 and 20 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, the Bates reference, the Krick reference, and further in view of U.S. Patent No. 5,633,878 to Ernkell et al. (the Ernkell reference). The Examiner rejected claims 6 and 21 under 35 U.S.C. § 103(a) as being obvious over the

Gillingham reference, the Bates reference, the Krick reference, and further in view of U.S. Patent No. 5,835,936 to Tomioka et al. (the Tomioka reference). The Examiner rejected claims 11 and 26 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, and further in view of the Krick reference. The Examiner rejected claims 12 and 27 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, the Krick reference, and further in view of the McAlpine reference. The Examiner rejected claims 13 and 28 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, the Krick reference, and further in view of the Ernkell reference. The Examiner rejected claims 14 and 29 under 35 U.S.C. § 103(a) as being obvious over the Gillingham reference, the Krick reference, and further in view of the Tomioka reference. The Examiner rejected claims 31, 32, 33, 36, 38, 39, 40, 41, 42, 45, and 47 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,415,403 to Huang et al. (the Huang reference), in view of U.S. Patent No. 5,946,247 to Osawa et al. (the Osawa reference). The Examiner rejected claims 34 and 43 under 35 U.S.C. § 103(a) as being obvious over the Huang reference, the Osawa reference, and further in view of U.S. Patent No. 6,058,056 to Beffa et al. (the Beffa reference). The Examiner rejected claims 35 and 44 under 35 U.S.C. § 103(a) as being obvious over the Huang reference, the Osawa reference, and further in view of U.S. Patent No. 6,019,501 to Okazaki (the Okazaki reference). The Examiner rejected claims 37 and 46 under 35 U.S.C. § 103(a) as being obvious over the Huang reference, the Osawa reference, and further in view of U.S. Patent No. 5,883,843 to Hii et al. (the Hii reference). The Examiner rejected claims 48-51 and 53 under 35 U.S.C. § 103(a) as being obvious over the Huang reference, in view of the Osawa reference, the Beffa

reference, and the Okazaki reference. The Examiner rejected claim 52 under 35 U.S.C. § 103(a) as being obvious over the Huang reference, the Osawa reference, the Beffa reference, the Okazaki reference, and further in view of the Hii reference. These rejections are respectfully traversed.

The present invention relates to a memory component, such as a DRAM device or a buffer device, residing within a memory module, having built-in self test. The memory component includes an input/output interface having a loopback. A controller is provided to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface. A compare register is provided to compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface. The memory module in which the memory component resides includes a plurality of memory devices and at least one buffer.

Independent claim 1, as amended, recites:

> an input/output interface having a loopback;
>
> a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and
>
> a compare register to compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface, *wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer.*

The Gillingham reference is directed to a semiconductor device having a self test circuit that includes an embedded dynamic random access memory array for storing data. A self test controller is provided for internally generating test data patterns and expected resulting data, and for comparing the expected resulting data with actual resulting data. Test interface circuitry is provided for loading the test data patterns into the memory and reading back the actual resulting data from the memory. A programming circuit is provided for selectively programming a voltage level to be applied to a selected cell plate of the memory according to predetermined test requirements, and a storage circuit is provided for storing an address of a defective memory cell.

The Gillingham reference does not disclose, teach, or suggest the memory component of independent claim 1, as amended. As already acknowledged by the Examiner, the Gillingham reference "does not explicitly teach the specific use of a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and a compare register to compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface" (Office Action, page 4, paragraph No. 4). Moreover, unlike the memory component of independent claim 1, as amended, the Gillingham reference does not disclose that *the memory component resides within a memory module having a plurality of memory devices and at least one buffer*. The Gillingham reference shows that the BIST controller (23) is *external* of the memory module (21) that contains the memory component (DRAM) (38) therein (col. 2, line 49-60; col. 3, lines 35-55; and Fig. 2). In

other words, a *memory component* with built-in self test having an *input/output interface*, a *controller*, and a *compare register*, wherein *the memory component resides within a memory module having a plurality of memory devices and at least one buffer*, as recited in independent claim 1, as amended, is different from the BIST system of the Gillingham reference in which the BIST controller is *external* to the memory module containing the memory component (DRAM) and *not* within the memory module.

The Bates reference, the Krick reference, the McAlpine reference, the Ernkell reference, and the Tomioka reference, alone or in combination, do not make up for the deficiencies of the Gillingham reference. In short, none of the Bates reference, the Krick reference, the McAlpine reference, the Ernkell reference, and the Tomioka reference discloses, teaches, or suggests a *memory component* with built-in self test having an *input/output interface*, a *controller*, and a *compare register*, wherein *the memory component resides within a memory module having a plurality of memory devices and at least one buffer*, as recited in independent claim 1, as amended. Accordingly, applicants respectfully submit that independent claim 1, as amended, distinguishes over the above-cited references.

Independent claims 9, 16, and 24, all as amended, recite limitations similar to independent claim 1, as amended. Claims 2-8 all depend, directly or indirectly, from independent claim 1, as amended. Claims 10-15 all depend, directly or indirectly, from independent claim 9, as amended. Claims 17-23 all depend, directly or indirectly, from independent claim 16, as amended. Claims 25-30 all depend, directly or indirectly, from independent claim 24, as amended. Accordingly, applicants respectfully submit

that claims 2-30 distinguish over the above-cited references for the reasons set forth above with respect to independent claim 1, as amended.

Independent claim 31, as amended, recites:

> a *plurality of memory components*;
>
> an address and command buffer adapted to transmit address and command data and test data to one of the plurality of memory components, wherein the address and command buffer includes a register to receive a test result; and
>
> at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the one of the plurality of memory components, and to compare the test data received from the address and command buffer with the test data received from the one of the plurality of memory components to generate the test result, wherein *the plurality of memory components, the address and command buffer, and the at least one data buffer all reside within the memory module*.

The Huang reference is directed to a built-in self test (BIST) for an embedded memory. A BIST controller includes a finite state machine used to step through a test sequence and control a sequence controller. The sequence.controller provides data and timing sequences to the embedded memory to provide page mode and non-page mode tests along with a refresh test. The BIST logic is scan-tested prior to performing the built-in self test and accommodations for normal memory refresh is made throughout the testing. The BIST also accommodates a burn-in test where unique burn-in test sequences can be applied.

The Huang reference does not disclose, teach, or suggest the memory module of independent claim 31, as amended. As already acknowledged by the Examiner, "Huang et al. do not explicitly teach the specific use of a register to receive a test result" (Office Action, page 12, line 10). Moreover, unlike the memory module of independent claim 31, as amended, the Huang reference does not make any mention of a *memory module* with built-in self test having a *plurality of memory components*, an *address and command buffer*, and *at least one data buffer*, wherein *the plurality of memory components, the address and command buffer, and the at least one data buffer all reside within the memory module*. The Huang reference only teaches a BIST chip component (10) with a single embedded memory component (DRAM) (13) (col. 4, lines 11-37; and Fig. 1), and there is no mention of a *memory module* having a *plurality of memory components*, *wherein the plurality of memory components, the address and command buffer, and the at least one data buffer all reside within the memory module*, as recited in independent claim 31, as amended.

The Osawa reference does not make up for the deficiencies of the Huang reference. The Osawa reference is directed to a testing device for making a functional test on a semiconductor memory that is a logic integrated circuit including a plurality of RAMs, a plurality of ROMS, and the like.

The Osawa reference does not disclose, teach, or suggest the memory module of independent claim 31, as amended. Unlike the memory module of independent claim 31, as amended, the Osawa reference does not disclose a *memory module* with built-in self test having a *plurality of memory components*, an *address and command buffer*, and *at least one data buffer*, wherein *the plurality of memory components, the*

address and command buffer, and the at least one data buffer all reside within the memory module. The Osawa reference only teaches a self test circuit (702) that controls a register circuit (706) to receive test results from a RAM test conducted by the self test circuit (702) (col. 77, lines 62-64; and Fig. 142). Accordingly, applicants respectfully submit that independent claim 31, as amended, distinguishes over the above-cited references.

The Beffa reference, the Okazaki reference, and the Hii reference, alone or in combination, do not make up for the deficiencies of the Huang reference and/or the Osawa reference. In short, none of the Beffa reference, the Okazaki reference, and the Hii reference discloses, teaches, or suggests a *memory module* with built-in self test having a *plurality of memory components*, an *address and command buffer*, and *at least one data buffer*, wherein *the plurality of memory components, the address and command buffer, and the at least one data buffer all reside within the memory module*, as recited in independent claim 31, as amended. Accordingly, applicants respectfully submit that independent claim 31, as amended, distinguishes over the above-cited references.

Independent claims 39 and 48, both as amended, recite limitations similar to independent claim 31, as amended. Claims 32-38 all directly depend from independent claim 31, as amended. Claims 40-47 all depend, directly or indirectly, from independent claim 39, as amended. Claims 49-53 all directly depend from independent claim 48, as amended. Accordingly, applicants respectfully submit that claims 32-53 distinguish over the above-cited references for the reasons set forth above with respect to independent claim 31, as amended.

Applicants believe that the foregoing amendments place the application in condition for allowance, and a favorable action is respectfully requested. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call either of the undersigned attorneys at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the Examiner believe that such a telephone conference would advance prosecution of the application.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1, 9, 16, 24, 31, 39, and 48 as follows:

1. (Amended) A memory component with built-in self test, comprising:

an input/output interface [coupled to the memory array and] having a loopback;

a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and

a compare register to compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

9. (Amended) A memory component with built-in self test, comprising:

a memory array;

an input/output interface coupled to the memory array and having a loopback;

a controller to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from the memory array; and

a compare register to compare the memory array test data transmitted to

the memory array with the memory array test data read from the memory array, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

16. (Amended) A method of testing a memory component with built-in self test, comprising:

transmitting input/output test data to an input/output interface having a loopback;

receiving the input/output test data from the loopback of the input/output interface; and

comparing the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface, wherein the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

24. (Amended) A method of testing a memory component with built-in self test, comprising:

transmitting memory array test data to a memory array;

storing the memory array test data in the memory array

reading the memory array test data from the memory array; and

comparing the memory array test data transmitted to the memory array with the memory array test data read from the memory array, wherein the memory component resides within a memory module having a plurality of

memory devices and at least one buffer.

31. (Amended) A memory module with built-in self test, comprising:

[at least one memory component] a plurality of memory components;

an address and command buffer adapted to transmit address and command data and test data to one of the [at least one memory component] plurality of memory components, wherein the address and command buffer includes a register to receive a test result; and

at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the [at least one memory component] one of the plurality of memory components, and to compare the test data received from the address and command buffer with the test data received from the [at least one memory component] one of the plurality of memory components to generate the test result, wherein the plurality of memory components, the address and command buffer, and the at least one data buffer all reside within the memory module.

39. (Amended) A method of testing a memory module with built-in self test, the method comprising:

transmitting address and command data and test data to a memory component among a plurality of memory components from an address and command buffer, wherein the plurality of memory components and the address and command buffer all reside within the memory module;

receiving the test data from the address and command buffer;

receiving the test data from the memory component; and

comparing the test data received from the address and command buffer with the test data received from the memory component to generate a test result.

48. (Amended) A memory module with built-in self test, comprising:

[at least one memory component] a plurality of memory components;

an address and command buffer adapted to transmit address and command data and test data to one of the [at least one memory component] plurality of memory components, wherein the address and command buffer includes,

a register to receive a test result,

a clock multiplier to receive a clock signal and to multiply the clock signal for transmission, and

an address and command generator to generate the address and command data; and

at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the [at least one memory component] one of the plurality of memory components, and to compare the test data received from the address and command buffer with the test data received from the [at least one memory component] one of the plurality of memory components to generate the test result, wherein the plurality of memory components, the address and command buffer, and the at least one data buffer

all reside within the memory module.